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CSP, INC.
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Burlington, Massachusetts 01803

To:

MARK MILLER
PROJECT XANADU
1213 MANOA RD
PHILADELPHIA PA 19151

MAP Array Processor

MAP

A New Series of Ultra-Fast, Programmable, Floating Point Array Processors

csp CSP Inc.

The Leader in Digital Signal Processing

- **15 Million Properly Rounded 32-Bit Floating Point Operations Per Second**
- **Assembly Language & Fortran Programmable**
- **Interfaces Provided for Popular Computers**
- **Field Upgradable**
- **Cost Effective**

~1979

MAP — the economic answer to accurate array processing in diverse applications . . .

• Seismic • Radar • Sonar • Telemetry • Biomedical • X-Ray • Image Processing

• Communications & Speech • Nuclear Science • Vibration & Noise Analysis • Simulation

CSP Inc.

MAP

Macro Arithmetic Processors

The New Generation of Programmable Processing Peripherals . . .

Reliable, ultra-fast array processing, at a reasonable cost, is here now!

The MAP series of floating-point signal processors and vector boxes brings a new dimension to real-time array processing . . . greatly increasing the processing speed and computation power of mini-computers and large computers.

These economical, small systems offer big performance advantages.

Super-fast total throughput

Unique overlapping of input, output, arithmetic, and executive operations, without speed penalties, for the ultimate in throughput speed.

Rapid accessing of large IC memory

Optimized efficiency by direct, simultaneous addressing — in bytes, half-words, and full word increments — of the 256Kbytes memory on each of three independent, asynchronous operating busses.

Accuracy over a wide dynamic range

32-bit hexadecimal floating point format properly rounded. No truncation. None of the usual noise or scaling problems.

Simple operation, with significant programming savings

Assembly language programmable, with complete signal processing software callable in Fortran. Easy writing of instructions due to program modularization. No rewrites or reassembling for changes in data structure or addressing.

Unusual versatility

Outstanding for handling FFTs, normal move-out, polynominal evaluation, integral equations, digital filtering running averages and medians . . . and a full spectrum of other algorithms. Uncompromised speed, efficiency, and accuracy.

MAP provides unmatched price/performance for any array processing requirements, with a full range of models to meet your specific data processing and analysis needs.

Typical Timing *All calculations in 32-bit floating point.*	**Extremely Efficient Signal Processors** *with their own internal processor for handling executive functions, freeing host computer for higher level tasks*		
	MAP-100	**MAP-200**	**MAP-300**
1024 Real FFT	30m Sec	7m Sec	2.8m Sec
1024 Complex FFT	60m Sec	12m Sec	4.5m Sec
Vector Fixed to Floating, Floating to Fixed — 1024 Components	1.5μ Sec	.25μ Sec	.25μ Sec
Complex Multiply (1024 Components)	7μ Sec	1.75μ Sec	.85μ Sec
Self Conjugate Multiply (1024 Components)	3.5μ Sec	1.0μ Sec	.45μ Sec
1024 pt. Correlation or Convolution with 32 pt. Kernal	55m Sec	14.0m Sec	7.0m Sec
Vector Compare & Replace (1024 Components	1.5m Sec	.5m Sec	.5m Sec
Recursive Filter Stage (per sample) 2nd Degree (2 poles + 2 zeros)	10μ Sec	2.0μ Sec	.85μ Sec

Powerful SNAP II Software

This unique multiprocessor scheduling and control system, loaded onto one of the memory busses (Standard Series), provides a one-step procedure for initiating complex, real-time mathematical analyses. Basic operations as well as sequences of previously programmed operations can be called with just one command . . . And, by having these available as simple Fortran commands, programming and operating times can be reduced by as much as 90%.

- Largest library of linear and non-linear commands offered for any processor (over 60 array functions)
- Sizeable selection of data management routines
- Data packing/unpacking routine
- Read/write and external buffer transfer control
- Definition, storage, and call of application programs
- Conditional execution capability
- Debugging programs
- Provision for addition and linking of user's algorithms or updating current commands by user
- Utility programs, with cross-assemblers and cross-emulators

User-Oriented

Further significant reductions in programming time and costs are achieved through the unusual programming simplicity offered by the Standard Series and the "V" Series.

- Assembly language programmable, eliminating error-prone microcoding and detail — no synchronization problems
- Modularized program structure, with addressing and arithmetic programs executed concurrently
- Special binding procedures — one addressing program can service up to 12 arithmetic programs
- One-word instructions — MAX and MIN functions are standard allowing users to accomplish in one instruction what normally requires 5 or more instruction loops in other systems

Each MAP system consists of several programmable processing elements, up to 768Kbytes of high-speed memory (125nSec bipolar and/or 500nSec MOS), and peripherals.

The MAP Standard Series (shown below)– the most powerful array processing peripherals, featuring internal control of executive functions for sequencing processing routines and adaptive program changes.

The MAP "V" Series — effective where specific algorithms with specific parameters are required to process data, operating under host computer control, with array command library stored in the host and transferred to the MAP as necessary.

Exclusive Multiprocessor Architecture

This special asynchronous CSPI-developed structure permits ultrafast throughput rates on a full range of mathematical functions.

Central Systems Processing Unit (CSPU) — acts as an internal controller (Standard Series)

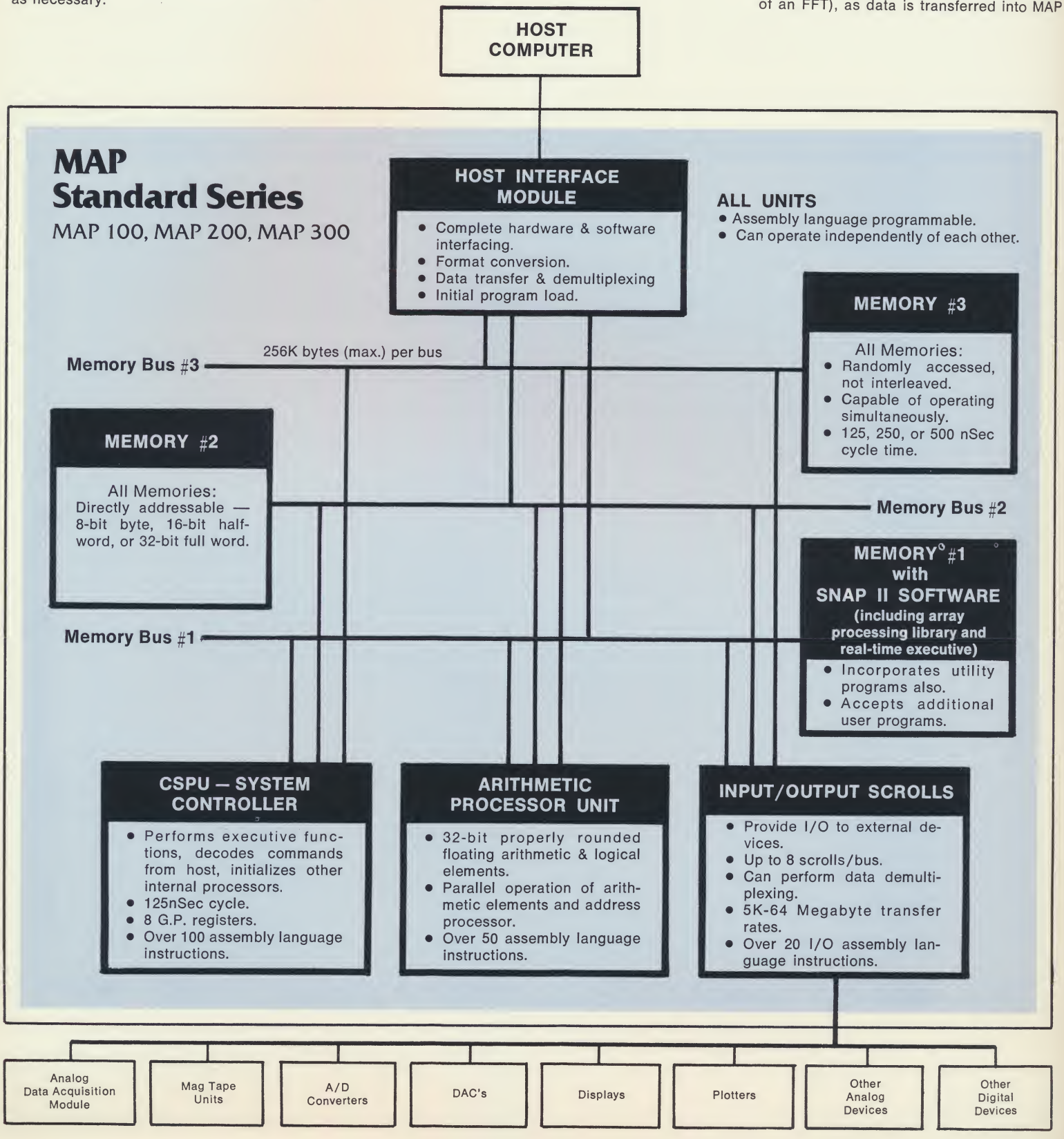
- Interprets host commands and links parameters
- Loads programs to appropriate processors from the MAP internally stored library
- Executes lists of signal processing functions without host computer supervision
- Performs miscellaneous computations and logic operations

Three Completely Independent Memories

- Parallel operation on separate programs possible
- I/O, arithmetic, and executive functions performed concurrently without cycle stealing
- Array commands stored on one memory bus (Standard Series)

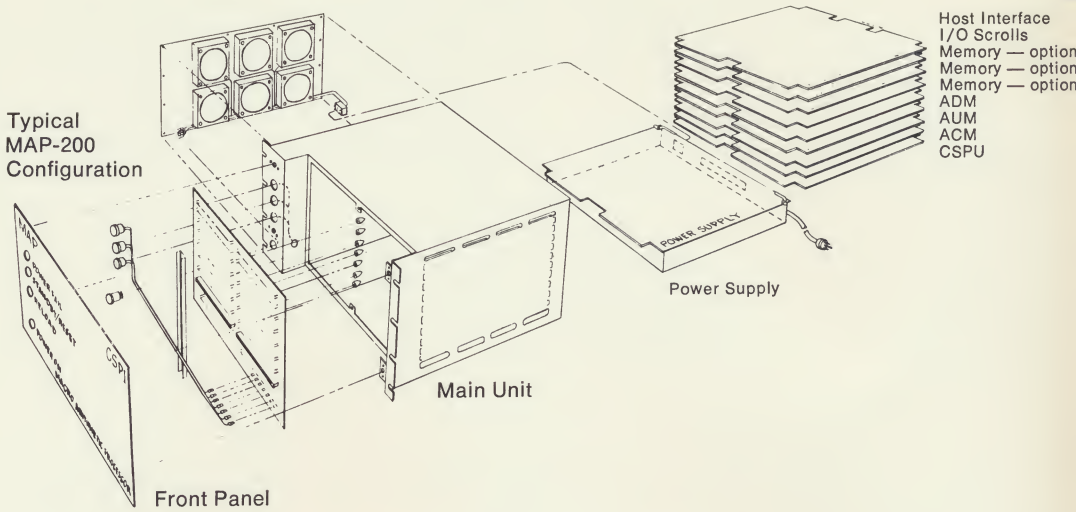
I/O Scrolls®

- Interface between MAP and external devices for maximum transfer efficiency.
- Memory used for only one cycle/transfer
- Relieves host computer from data acquisition or data output and display tasks
- Demultiplex data and perform complex operations (including bit reversal addressing of an FFT), as data is transferred into MAP



MAP

- Rugged
- Reliable
- Field Upgradeable



Simple Maintenance

- Multiwire and PC boards and PC bus backplane for easy card-level maintenance
- Extensive diagnostic routines for quick fault isolation to PC card

No Obsolescence Problems

- All MAP models — field expandable, in hardware and software
- No slot sensitivity as well as asynchronous design — allows plug-in of additional arithmetic cards for increased performance capabilities
- Memory speed or capacity changes possible on each of the 3 busses
- Up to 24 I/O Scrolls available for increased communications with more external I/O devices

MAP-100
Excellent general purpose system with a high-speed arithmetic unit for all mathematical operations

MAP-200
Increased capability with a separate multiplier and adder, able to operate in parallel

MAP-300
Optimum performance of mathematically intensive operations through use of 2 multipliers and 2 adders

MAP V-20 and V-30
Rapidly perform fixed algorithms with the precision of the MAP-200 and MAP-300. These more economical vector processors require more host computer control.

Militarized versions of MAP (complying with MIL-E-16400 and MIL-E-5400) are available.

Software:

Operational:	SNAP II Executive (Simple Notation for Array Processing) SNAP II Library — over 60 array processing algorithms
Utility:	Hardware diagnostics, Loader, Debug package, Cross-assembler and emulator in Fortran, I/O drivers for most mini's and maxi's

Environmental:

Temperature:	0-50°C
Humidity:	10-90% (no condensation)
Voltage:	115/230 single phase ±10%
Frequency:	47-63 Hz
Power:	400 watts (typical)
Weight:	80 lbs. (typical)

MAP — the powerful, easy-to-use peripheral — enhances and expands the performance of any computer system.

CSP Inc. — the leader in digital signal processing — has been a problem-solving organization since 1968. The company, the first to be organized expressly to develop and manufacture advanced, practical digital signal processing turnkey systems, has a proven record of accomplishments . . . in hardware, software, and applications assistance. Over 100 of these super-fast CSPI signal processing systems are in use in the field.

In 1970, CSP Inc. delivered the 16-bit CSP-30 computer with a 100nSec cycle time — still the world's fastest minicomputer. SNAP I was on-stream in 1970. Interleaved, ported, and half-cycled memories were standard for CSP Inc. systems in 1971. The 4001 Array Processor, on the market in 1972, introduced microprogrammability. The MAP Series of Macro Arithmetic Processors, announced in 1974, is the latest "breakthrough." This new generation of easily programmable, ultra-fast floating point processors incorporates complete internal software control.

These innovative CSP Inc. systems are in use in a broad range of industrial companies and government agencies. Among these are: GE, Westinghouse, Singer, Philco-Ford, RCA, General Dynamics, Computer Sciences Corp., Bell Labs, and major Government laboratories.

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